WHAT IS CLAIMED IS:

1. An RACH receiving apparatus for demodulating a reception signal spread-spectrum by long codes, phase rotation information, and signatures, the apparatus comprising:

a first multiplying unit for multiplying said reception signal by first despreading codes operated by the long codes and phase rotation information;

a first adding unit for adding a plurality of multiplication results outputted from said first multiplying unit at specific intervals;

a second multiplying unit for multiplying a plurality of addition results outputted from said first adding unit by second despreading codes of the signatures; and

a second adding unit for adding multiplication results outputted from said second multiplying unit to obtain correlation outputs.

2. The apparatus according to claim 1, comprising a complex operating unit for performing a complex operation to the correlation outputs generated from the second adding unit.

3. The apparatus according to claim 1, wherein a complex operating unit for performing a complex operation to the reception signal is provided between the first adding

unit and the second multiplying unit.

4. An RACH receiving apparatus for demodulating a reception signal spread-spectrum by long codes, phase rotation information, and signatures, the apparatus comprising:

a complex operation processing unit for performing a complex operation processing to the reception signal;

a first multiplying unit for multiplying an in-phase component and a quadrature component in said complex operation result by first despreading codes of the long codes;

a first adding unit adding a plurality of multiplication results of the in-phase component and the quadrature component outputted from said first multiplying unit at specific intervals;

a second multiplying unit for multiplying a plurality of addition results outputted from said first adding unit by second despreading codes of the signatures; and

a second adding unit for adding multiplication results outputted from the second multiplying unit to obtain correlation outputs.

5. The apparatus according to claim 3, wherein said first multiplying unit multiplies the in-phase component and the quadrature component in the reception signal by the first

despreading codes in a time-division manner at a speed that is integer times as high as a sampling speed of an input signal, and the first adding unit performs the addition at said integer-times speed.

6. The apparatus according to claim 4, wherein the first multiplying unit multiplies the in-phase component and the quadrature component in the reception signal by the first despreading codes in a time-division manner at a speed that is integer times as high as a sampling speed of an input signal, and the first adding unit performs the addition at said integer-times speed.

7. The apparatus according to claim 5, wherein the second multiplying unit performs the multiplication of the inputted operation results and the second despreading codes at a speed increased by times corresponding to the number of kinds of the second despreading codes and the second adding unit performs the addition at the speed increased by times corresponding to the number of kinds of the second despreading codes.

8. The apparatus according to claim 6, wherein the second multiplying unit performs the multiplication of the inputted operation results and the second despreading codes at a speed increased by times corresponding to the number of kinds of the second despreading codes and the second adding unit performs the addition at the speed increased by times

corresponding to the number of kinds of the second despreading codes.

9. The apparatus according to claim 7, wherein the first multiplying unit performs the multiplication of the in-phase component and the quadrature component in the reception signal and the first despreading codes in such a time-division manner that capture timing of the in-phase component and the quadrature component is set to a speed that is integer times as high as a sampling speed of an input signal and, on the other hand, capture timing of the first despreading code is set to a speed that is twice as high as the speed, and the first adding unit performs the addition at the speed that is twice as high as the integer-times speed.